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| 10/727,181 | 12/02/2003 | Richard Thomas Plunkett | PEA01US | 6713 |

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| EXAMINER | |
|---|---|
| KAU, STEVEN Y | |

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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/727,181 | PLUNKETT ET AL. | |
| | Examiner | Art Unit | |
| | STEVEN KAU | 2625 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *04 January 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-6* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 June 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

# DETAILED ACTION

### *Continued Examination Under 37 CFR 1.114*

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on January 4, 2009 has been entered.

### *Response to Amendment*

2. Applicant's amendment was received on 1/4/2009, and has been entered and made of record. Currently, claim 6 is added and claims 1-6 are pending for further examination in this Action.

### *Response to Remark/Arguments*

3. Applicant's arguments with respect to claims 1-5 have been fully considered and the reply to the Remarks/Arguments is in the following:

- Applicant's arguments with respect to claims 1-5 have been fully considered but are moot in view of the new ground(s) of rejection.

- Applicant's arguments, section "Claim Objection" in page 6, Remarks with respect to claim 5 is persuasive. Claim objection of lacking proper antecedent basis has been withdrawn from the record.
- Applicant is remind to comply with 37 U.S.C. 1.173(c), which requires that "Whenever there is an amendment to the claim pursuant to paragraph (b) of this section, there must also be supplied, on pages separate from the pages containing the changes, the status (i.e. pending or canceled), as of the date of the amendment, of all patent claims and of all added claims, and an explanation of the support in the disclosure of the patent for the changes made to the claims".

## *Claim Rejections - 35 USC § 103*

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shu (US 5,594,839) in view of Hirahara et al (US 4,910,603) and Hashimoto (US 4,999,814).

Regarding claim 1.

Claim 1 is directed to a method claim for sequentially outputting full lines of dither values of a dither matrix stored in a memory to a buffer memory involving reading a plurality of dither values, updating the start position in the memory, and outputting the full line of dither values, etc. The method claim does not specifically mention which type of machine is used to perform such steps. The examiner considers that all active steps of the method must be executed by a particular machine, i.e. a computer with dithering process software so that such steps can be performed. Thus, this method claim satisfies 35 U.S.C. 101 statutory requirements.

Hirahara discloses a method for sequentially outputting full lines of dither values of a dither matrix stored in a memory (**e.g. dither process for image reproduction and full lines of dither value are outputted from a memory, e.g. memory 738 of Fig. 7 in a sequential order, i.e. lines of dither value is controlled by pixel address, col 10, lines 15-34**), comprising the steps of:

(a) reading a plurality of dither values of the dither matrix from the memory into a buffer memory (**referring to Fig. 7, dither values are outputting to buffer memory 710**), the reading commencing at a start position in the memory until a full line of dither values of the dither matrix has been read (**i.e. identifying a line in the dither array with address for halftone process; thus each time a line is retrieved from ROM, a start position of the line in the ROM is adjusted, or commenced, col 10, lines 23-44**);

(b) updating the start position to an updated start position in the memory of a subsequent line of dither values (**e.g. since more than one dither lines are stored in the dither array, thus the next to the current line being processed must be**

**updated to be a new line in order to continue for halftone processing, col 10, lines 35-48**);

(e) repeating steps (a) - (c) until all lines of dither values of the dither matrix have been read and output to the buffer memory (**e.g. halftone processing is perform pixel by pixel; in addition, dither array is smaller than the image array and during dither process, dither array is repeated side by side over the image array to produce repetitive pattern, thus iteration of steps (a) to (c) must be performed**, **col 8, lines 10-23**).

Shu does not disclose (c) outputting the full line of dither values into the buffer memory; (d) outputting a full line of dither values from the buffer memory, said outputting of dither values from the buffer memory commencing after a full line of dither values has been output into the buffer memory; and wherein after a first iteration of steps (a) - (c), steps (a) to (c) are performed simultaneously with step (d).

Hirahara teaches (c) outputting the full line of dither values into the buffer memory (**i.e. 6-bit serial output of Dither matrix in ROM 22 is sent to buffers 25 and 26, and is controlled by line counter 23, Fig. 8, col 7, lines 46-60**); (d) outputting a full line of dither values from the buffer memory (**i.e. the buffer 25 and 26 are two-line buffer and these buffers are alternately access for writing and reading, Col 7, 57-67 and Fig. 9**), said outputting of dither values from the buffer memory commencing after a full line of dither values has been output into the buffer memory (**i.e. since the operation described above is controlled by line counter 23 of Fig. 8, and giving the fact that buffers 25 and 26 are two-line buffer and are accessed alternately by**

**writing and reading; thus, each line of dither values in and out the buffers must satisfy the above limitation, col 7, lines 46-67**); and

Hashimoto teaches wherein after a first iteration of steps (a) - (c), steps (a) to (c) are performed simultaneously with step (d) (**i.e. simultaneous generation of write, read and refresh can be achieved for read/write line buffer memory, col 6, lines 31-40**).

Having a method of Shu' 839 reference and then given the well-established teaching of Hirahara' 603 reference, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the method of Shu' 839 reference to include (c) outputting the full line of dither values into the buffer memory; (d) outputting a full line of dither values from the buffer memory, said outputting of dither values from the buffer memory commencing after a full line of dither values has been output into the buffer memory as taught by Hirahara' 603 reference since doing so would increase the versatility of the method; and then to modify the combination of Shu and Hirahara to include wherein after a first iteration of steps (a) - (c), steps (a) to (c) are performed simultaneously with step (d) as taught by Hashimoto' 814, since doing so would improve the method efficiency and save process time, and further the services provided could easily be established for one another with predictable results.

Regarding claim 6, in accordance with claim 1.

Shu does not disclose wherein step (d) is performed at a rate faster than step (a).

Hashimoto teaches wherein step (d) is performed at a rate faster than step (a) (**i.e. read/write control of DRAM has been a task, i.e. Fig. 21 of the specification of**

**the current application, and Hashimoto discloses that assuming 30 nsec for maximum bit rate for serial data writing or reading and 300 nsec for cycling, thus, outputting one full line from a buffer is for sure faster than step (a) of the current invention, col 3, lines 1-36**).

Having a method of Shu' 839 reference and then given the well-established teaching of Hashimoto' 814 reference, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the method of Shu' 839 reference to include wherein step (d) is performed at a rate faster than step (a), since doing so would have improve the control of data processing in between memories and buffers.

6. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Shu (US 5,594,839) (Shu' 839) in view of Hirahara et al (US 4,910,603) and Hashimoto (US 4,999,814) as applied to claim 1 above, and further in view of Young et al (US 6,154,195).

Regarding claim 4, in accordance with claim 1.

Shu' 839 does not disclose wherein, in repeated step (b), it is determined whether dither values at an end position in the memory have been read, and if so, the updated start position is updated to the initial start position.

Young' 195 teaches wherein, in repeated step (b), it is determined whether dither values at an end position in the memory have been read, and if so, the updated start position is updated to the initial start position (**Young' 195 teaches outputting dither**

**values to a buffer memory line by line in step (b), thus, the end of each line must be determined and a new line must be updated in order to have the halftone process performed properly, Fig. 3, col 7, lines 47-50**).

Having a method of sequentially outputting full lines of dither values of a dither matrix of Shu' 839 reference and then given the well-established teaching of Young' 195 reference, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the method of Shu' 839 reference to include in repeated step (b), it is determined whether dither values at an end position in the memory have been read, and if so, the updated start position is updated to the initial start position as taught by Young' 195 reference since doing so would ensure the dither/half-tone performed properly and further outputting dither values to a buffer memory and updating line input provided by Young' 195 could easily be established for one another with predictable results.

7. Claims 2 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shu (US 5,594,839) (Shu' 839) in view of Hirahara et al (US 4,910,603) and Hashimoto (US 4,999,814) as applied to claim 1 above, and further in view of Yamashita et al (US 5,701,505).

Regarding claim 2, in accordance with claim 1.

Shu does not explicitly disclose wherein a plurality of dither matrices are stored in the memory, and wherein step (a) includes reading a plurality of dither values from at least two of the dither matrices simultaneously.

Yamashita discloses wherein a plurality of dither matrices are stored in the memory (**e.g. dither matrices are contained in the halftone circuits, which implies that dither matrices are stored in the memory of the circuitry, col 20, line 43 through col 21, line 11**), and wherein step (a), includes reading a plurality of dither values from at least two of the dither matrices simultaneously (**e.g. Yamashita discloses a parallel processing apparatus which processing data in block cycles, i.e. Fig. 27 teaches a process of outputting 4 lines; in order to support the parallel processing, the halftone-processing circuits 751-754 must reading at least two of the dither matrices simultaneously as shown in Figs 32-25 & col 20, line 63 through col 21, line 11**).

Having a method of sequentially outputting full lines of dither values of a dither matrix of Shu' 839 reference and then given the well-established teaching of Yamashita' 505 reference, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the combination of Shu' 839, Hirahara' 603 and Hashimoto' 814 to include a plurality of dither matrices are stored in the memory, and wherein step (a) includes reading a plurality of dither values from at least two of the dither matrices simultaneously as taught by Yamashita' 505 reference since doing so would improve processing efficiency to reducing processing time, and further, the concept of parallelism can be implemented with a predictable result.

Regarding claim 5, in accordance with claim 2.

Claim 5 recites identical features as claim 4. Thus, arguments similar to that presented above for claim 4 are also equally applicable to claim 5.

8. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Shu (US 5,594,839) (Shu' 839) in view of Hirahara et al (US 4,910,603) and Hashimoto (US 4,999,814), and further in view of Yamashita et al (Yamashita) (US 5,701,505) as applied to claim 2 above, and further in view of Matsuba et al (Matsuba) (US 5,815,286).

Regarding claim 3, in accordance with claim 2.

Shu' 839 does not disclose wherein the dither matrices are of different sizes.

Matsuba' 286 discloses wherein the dither matrices are of different sizes (**e.g. four color components can be processed with respect to four threshold matrices value at the same time**, **Figs. 1a-c & col 7, lines 9-18 and col 20, lines 21-32**).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to have modified the combination of Shu' 839, Hirahara' 603, Hashimoto' 814 and Yamashita' 505 to include that dither matrices are of different sizes taught by Matsuba' 286 and therefore, four color components can be processed with respect to four threshold matrices value at the same time (Figs 21A-D, col 20, lines 21-32).

## *Conclusion*

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven Kau whose telephone number is 571-270-1120 and fax number is 571-270-2120. The examiner can normally be reached on M-F, 8:30am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Moore can be reached on 571-272-7437. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Steven Kau/
Examiner, Art Unit 2625
3/12/2009

/David K Moore/
Supervisory Patent Examiner, Art Unit 2625